

Amendment Under 37 C.F.R. § 1.116
U.S. Application No.: 09/909,910

The listing of claims will replace all prior versions, and listing, of claims in the application:

AMENDMENTS OF CLAIMS:

1. (Previously Presented) An AC plane discharge plasma display panel comprising:

a front substrate;

a rear substrate;

a sealing portion operable to encapsulate said front substrate and said rear substrate at a peripheral edge portion thereof to seal a discharge gas therein;

column ribs and row ribs operable to define pixel cells in a column direction and in a row direction, respectively, to thereby define the pixel cells in a matrix;

plane discharge electrodes provided on said front substrate having a display electrode portion and a bus electrode portion; and

a plurality of electrodes provided on said rear substrate which extend longitudinally in the column direction,

wherein the display electrode portion comprises sustain electrodes and scan electrodes and the bus electrode portion comprises sustain-side bus electrodes and scan-side bus electrodes,

wherein at least part of the display electrode portion has a notched portion or a cut-away portion between pixel cells adjacent to each other in the row direction, thereby providing each pixel cell with individually separated electrodes, and

Amendment Under 37 C.F.R. § 1.116
U.S. Application No.: 09/909,910

wherein a single sustain electrode is provided in common for a first and second pixel cell adjacent to each other in the column direction.

2. (Original) The plasma display panel according to claim 1, wherein neighboring sustain electrodes or sustain-side bus electrodes for neighboring pixel cells arranged in the column direction are electrically connected to each other in the panel.

3. (Original) The plasma display panel according to claim 1, wherein neighboring scan electrodes or scan-side bus electrodes for neighboring pixel cells arranged in the column direction are electrically connected to each other in the panel.

4. (Previously Presented) A method for fabricating the plasma display panel of claim 1, comprising the steps of:
encapsulating said rear substrate and said front substrate in a vacuum, and
sealing a discharge gas in the panel continually thereafter without exposing the interior of the panel to the atmosphere.

5. (Previously Presented) The plasma display panel according to claim 1, wherein said column ribs and row ribs form lattice-shaped ribs and are provided on said rear substrate.

6. (Original) The plasma display panel according to claim 5, wherein a gap for allowing a discharge gas to pass therethrough is provided between the top of the lattice-shaped rib and said front substrate.

7. (Original) The plasma display panel according to claim 6, further comprising projected portions provided on intersections of lattice-shaped ribs of said front substrate or said rear substrate, said intersections corresponding to those of lattice-shaped ribs of said rear substrate.

8. (Original) The plasma display panel according to claim 7, wherein said projected portions define scan-side bus electrodes and sustain-side bus electrodes or scan electrodes and sustain electrodes between pixel cells adjacent to each other in the row direction.

9. (Original) The plasma display panel according to claim 6, further comprising recessed portions provided on intersections of lattice-shaped ribs of said front substrate or said rear substrate, said intersections corresponding to those of lattice-shaped ribs of said rear substrate.

10. (Original) The plasma display panel according to claim 9, further comprising rib portions other than said recessed portions defining at least scan electrodes and sustain electrodes between pixel cells adjacent to each other in the column direction.

11. (Previously Presented) The plasma display panel according to claim 6, further comprising horizontal barrier walls having a thickness of 2 to 50 μ m between pixel cells, said horizontal barrier walls being formed in parallel to the bus electrode portion.

12. (Previously Presented) The plasma display panel according to claim 11, wherein said horizontal barrier wall is formed of a material having a dielectric constant lower than that of an insulating layer provided on said front substrate.

13. (Previously Presented) The plasma display panel according to claim 11, wherein said horizontal barrier wall is placed only between the sustain-side bus electrodes.

14. (Previously Presented) The plasma display panel according to claim 11, wherein said horizontal barrier walls between the sustain-side bus electrodes and between the scan-side bus electrodes have different widths.

15. (Previously Presented) The plasma display panel according to claim 11, wherein the horizontal barrier walls are provided with an extended portion formed orthogonal to the longitudinal direction of the horizontal barrier wall, said extended portion being disposed between pixel cells adjacent to each other in the longitudinal row direction.

16. (Previously Presented) The plasma display panel according to claim 6, wherein said column ribs and row ribs form lattice-shaped ribs and are provided on the rear substrate, wherein a rib portion extending in the longitudinal row direction for defining pixel cells is higher than a rib portion extending in the longitudinal column direction for defining pixel cells.

17. (Previously Presented) The plasma display panel according to claim 11, wherein a pair of sustain-side bus electrodes or scan-side bus electrodes are not overlapped by the horizontal barrier but are overlapped by each of said ribs.

18. (Previously Presented) The plasma display panel according to claim 11, wherein a pair of sustain-side bus electrodes or scan-side bus electrodes is not overlapped by each of said ribs but is overlapped by the horizontal barrier.

19. (Previously Presented) The plasma display panel according to claim 11, wherein each of said ribs and the horizontal barrier overlap a pair of sustain-side bus electrodes or scan-side bus electrodes.

20. (Previously Presented) The plasma display panel according to claim 6, wherein the sustain-side bus electrodes and the scan-side bus electrodes have a thickness of 10 to 50 μ m, and the thickness of the sustain-side bus electrodes and the scan-side bus electrodes causes a raised

portion of thickness 2 to 50 μ m to be formed on the surface of an insulating layer provided on said front substrate.

21. (Previously Presented) The plasma display panel according to claim 1, comprising a metal electrode connecting the sustain-side bus electrodes to each other.

22. (Previously Presented) The plasma display panel according to claim 1, comprising a transparent electrode connecting the sustain-side bus electrodes to each other.

23. (Previously Presented) The plasma display panel according to claim 1, wherein the sustain-side bus electrodes are connected to each other to act as an integrated common bus electrode.

24. (Original) The plasma display panel according to claim 23, wherein resistance of the common bus electrode is 1/3 to 1/12 of that of the scan-side bus electrode.

25. (Previously Presented) The plasma display panel according to claim 23, wherein the common bus electrode has a thickness of 10 to 50 μ m, and the thickness of the common bus electrode causes a raised portion of thickness 2 to 50 μ m to be formed on the surface of an insulating layer provided on said front substrate.

Amendment Under 37 C.F.R. § 1.116
U.S. Application No.: 09/909,910

26. (Previously Presented) The plasma display panel according to claim 1, comprising a metal electrode connecting the scan-side bus electrodes to each other.

27. (Previously Presented) The plasma display panel according to claim 1, comprising a transparent electrode connecting the scan-side bus electrodes to each other.

28. (Previously Presented) The plasma display panel according to claim 1, wherein the scan-side bus electrodes are connected to each other to act as an integrated common bus electrode.

29. (Original) The plasma display panel according to claim 28, wherein resistance of the common bus electrode is $1/3$ to $1/12$ of that of the sustain-side bus electrode.

30. (Previously Presented) The plasma display panel according to claim 28, wherein the common bus electrode has a thickness of 10 to 50 μm , and the thickness of the common bus electrode causes a raised portion of thickness 2 to 50 μm to be formed on the surface of an insulating layer provided on said front substrate.

Amendment Under 37 C.F.R. § 1.116
U.S. Application No.: 09/909,910

31. (Original) The plasma display panel according to claim 1, wherein the distance between the neighboring scan electrodes or the neighboring scan-side bus electrodes on vertically neighboring pixel cells is 20 to 200 μ m.

32. (Original) The plasma display panel according to claim 1, wherein the distance between the neighboring sustain electrodes or the neighboring sustain-side bus electrodes on vertically neighboring pixel cells is 20 to 200 μ m.

33. (Original) The plasma display panel according to claim 1, wherein the scan electrodes of neighboring pixel cells overlap each other being electrically insulated.

34. (Original) The plasma display panel according to claim 1, wherein the sustain electrodes of neighboring pixel cells overlap each other being electrically insulated.

35. (Original) The plasma display panel according to claim 1, comprising a notched or cut-away end portion of a display electrode portion disposed in the row direction, said notched or cut-away end portion being spaced apart by 20 to 70 μ m from a head portion of a rib disposed in the column direction.

36. (Original) The plasma display panel according to claim 1, wherein the sustain electrode has a portion, reduced in width, for connecting to the sustain-side bus electrode.

37. (Previously Presented) The plasma display panel according to claim 1, wherein the plane discharge electrodes are constructed so as to allow pixel cells disposed in the longitudinal column direction to have centers of light emission at equal intervals.

38. (Previously Presented) The plasma display panel according to claim 1, comprising horizontal black stripes disposed in the row direction.

39. (Original) The plasma display panel according to claim 38, wherein said horizontal black stripes, all having the same width, are disposed at equal intervals in the column direction to be vertically symmetric with each other in each pixel cell.

40. (Previously Presented) The plasma display panel according to claim 38, wherein the horizontal black stripes overlap neighboring scan-side bus electrodes in the column direction, and wherein the horizontal black stripes and a common bus electrode have the same width and are disposed at equal intervals in the column direction.

41. (Previously Presented) The plasma display panel according to claim 38, wherein said scan electrodes and sustain electrodes are formed on said first substrate, and said horizontal black stripes are formed on the scan electrode and the sustain electrode.

42. (Previously Presented) The plasma display panel according to claim 41, wherein a hole or notch is formed on the horizontal black stripes to ensure electrical connection of the scan electrode or the sustain electrode to the bus electrode portion.

43. (Previously Presented) The plasma display panel according to claim 1, wherein the display electrode portion extends longitudinally in the column direction and the bus electrode portion extends longitudinally in the row direction.

44. (Previously Presented) The plasma display panel according to claim 1, wherein each pixel cell comprises a sustain electrode, a sustain-side bus electrode, a scan electrode, and a scan-side bus electrode.

45. (Previously Presented) The plasma display panel according to claim 1, wherein the sustain electrodes and the scan electrodes are disposed so as to allow respective sustain electrodes and scan electrodes to be adjacent to each other between neighboring pixel cells in the column direction.

46. (Previously Presented) A display panel comprising:

a first substrate;

a second substrate provided opposite said front substrate;

a display electrode portion provided on said first substrate and extending longitudinally in a first direction;

a bus electrode portion extending longitudinally in a second direction perpendicular to the first direction;

a plurality of electrodes provided on said second substrate and extending longitudinally in the first direction; and

ribs which define pixel cells in the first direction and the second direction, respectively, to thereby define pixel cells in a matrix,

wherein at least a part of the display electrode portion is provided in common for pixel cells adjacent to each other in the first direction.

47. (Canceled)

48. (Previously Presented) The display panel according to claim 46, wherein the display electrode portion comprises a sustain electrode and a scan electrode, and the bus electrode portion comprises a sustain-side bus electrode and a scan-side bus electrode.

49. (Canceled)

50. (Previously Presented) The display panel according to claim 48, wherein the sustain electrode is the part of the display portion provided in common for pixel cells adjacent to each other in the first direction.

51. (Previously Presented) The display panel according to claim 48, wherein a gap is formed in the first direction within each pixel cell between the sustain electrode and the scan electrode.

52. (Previously Presented) An AC plane discharge plasma display panel comprising:
a front substrate;
a rear substrate;
a sealing portion for encapsulating said front substrate and said rear substrate at a peripheral edge portion thereof to seal a discharge gas therein;
column ribs and row ribs for defining pixel cells in a column direction and in a row direction, respectively, to thereby define the pixel cells in a matrix; and
plane discharge electrodes having a display electrode portion and a bus electrode portion, at least part of the display electrode portion of said plane discharge electrodes having a notched portion or a cut-away portion between pixel cells adjacent to each other in the row direction, said plane discharge electrodes having a pair of a sustain electrode and a scan electrode placed in one pixel cell, and for neighboring pixel cells arranged in the column direction, sustain electrodes

Amendment Under 37 C.F.R. § 1.116
U.S. Application No.: 09/909,910

and scan electrodes are disposed to allow respective sustain electrodes and scan electrodes to be adjacent to each other between neighboring pixel cells.

53-54. (Canceled)

55. (New) The plasma display panel according to claim 52, wherein neighboring sustain electrodes or sustain-side bus electrodes for neighboring pixel cells arranged in the column direction are electrically insulated from each other in each cell.

56. (New) The plasma display panel according to claim 55, wherein said neighboring sustain electrodes or sustain-side bus electrodes are electrically connected to each other in the panel.

57. (New) The plasma display panel according to claim 55, wherein said neighboring sustain electrodes or sustain-side bus electrodes are electrically insulated from each other in the panel.

58. (New) The plasma display panel according to claim 52, wherein neighboring scan electrodes or scan-side bus electrodes for neighboring pixel cells arranged in the column direction are electrically insulated from each other in each cell.

59. (New) The plasma display panel according to claim 58, wherein said neighboring scan electrodes or scan-side bus electrodes are electrically connected to each other in the panel.

60. (New) The plasma display panel according to claim 58, wherein said neighboring scan electrodes or scan-side bus electrodes are electrically insulated from each other in the panel.

61. (New) A method of fabricating the plasma display panel of claim 52, comprising the steps of:

encapsulating said rear substrate and said front substrate in vacuum, and sealing a discharge gas in the panel continually thereafter without exposing the interior of the panel to the atmosphere.

62. (New) The plasma display panel according to claim 52, wherein the scan electrodes of neighboring pixel cells overlap each other being electrically insulated.

63. (New) The plasma display panel according to claim 52, wherein the sustain electrodes of neighboring pixel cells overlap each other being electrically insulated.

64. (New) The plasma display panel according to claim 52, comprising a notched or cut-away end portion of a display electrode portion disposed in the row direction, said notched or cut-away end portion being spaced apart by 20 to 70 μ m from a head portion of a rib disposed in the column direction.

65. (New) The plasma display panel according to claim 52, wherein the sustain electrodes have a portion, reduced in width, for connecting to the sustain-side bus electrodes.

66. (New) The plasma display panel according to claim 52, comprising horizontal black stripes disposed in the row direction.

67. (New) The plasma display panel according to claim 66, wherein said horizontal black stripes, all having the same width, are disposed at equal intervals in the column direction to be vertically symmetric with each other in each pixel cell.

68. (New) The plasma display panel according to claim 66, wherein said scan electrodes and sustain electrodes are formed on said front substrate, and said horizontal black stripes are formed on the scan electrode and the sustain electrode.

69. (New) The plasma display panel according to claim 68, wherein a hole or notch is formed on the horizontal black stripes to ensure electrical connection of the scan electrode or the sustain electrodes to the bus electrode portion.

70. (New) The plasma display panel according to claim 52, wherein said column ribs and row ribs form lattice-shaped ribs and are provided on said rear substrate.

71. (New) The plasma display panel according to claim 70, wherein a gap for allowing a discharge gas to pass therethrough is provided between the top of the lattice-shaped rib and said front substrate.

72. (New) The plasma display panel according to claim 71, further comprising projected portions provided on intersections of lattice-shaped ribs of said front substrate or said rear substrate, said intersections corresponding to those of lattice-shaped ribs of said rear substrate.

73. (New) The plasma display panel according to claim 72, wherein said projected portions define scan-side bus electrodes and sustain-side bus electrodes or scan electrodes and sustain electrodes between pixel cells adjacent to each other in the row direction.

74. (New) The plasma display panel according to claim 71, further comprising recessed portions provided on intersections of lattice-shaped ribs of said front substrate or said rear substrate, said intersections corresponding to those of lattice-shaped ribs of said rear substrate.

75. (New) The plasma display panel according to claim 74, further comprising rib portions other than said recessed portions defining at least scan electrodes and sustain electrodes between pixel cells adjacent to each other in the column direction.

76. (New) The plasma display panel according to claim 71, further comprising horizontal barrier walls having a thickness of 2 to 50 μ m between pixel cells, said horizontal barrier walls being formed in parallel to the bus electrode portion.

77. (New) The plasma display panel according to claim 76, wherein said horizontal barrier wall is formed of a material having a dielectric constant lower than that of an insulating layer provided on said front substrate.

78. (New) The plasma display panel according to claim 76, wherein said horizontal barrier wall is placed only between the sustain-side bus electrodes.

79. (New) The plasma display panel according to claim 76, wherein said horizontal barrier walls between the sustain-side bus electrodes and between the scan-side bus electrodes have different widths.

80. (New) The plasma display panel according to claim 76, wherein the horizontal barrier walls are provided with an extended portion formed orthogonal to the longitudinal direction of the horizontal barrier wall, said extended portion being disposed between pixel cells adjacent to each other in the longitudinal row direction.

81. (New) The plasma display panel according to claim 71, wherein said column ribs and row ribs form lattice-shaped ribs and are provided on the rear substrate, wherein a rib portion extending in the longitudinal row direction for defining pixel cells is higher than a rib portion extending in the longitudinal column direction for defining pixel cells.

82. (New) The plasma display panel according to claim 76, wherein a pair of sustain-side bus electrodes or scan-side bus electrodes are not overlapped by the horizontal barrier but are overlapped by each of said ribs.

83. (New) The plasma display panel according to claim 76, wherein a pair of sustain-side bus electrodes or scan-side bus electrodes is not overlapped by each of said ribs but is overlapped by the horizontal barrier.

84. (New) The plasma display panel according to claim 76, wherein each of said ribs and the horizontal barrier overlap a pair of sustain-side bus electrodes or scan-side bus electrodes.

85. (New) The plasma display panel according to claim 71, wherein the sustain-side bus electrodes and the scan-side bus electrodes have a thickness of 10 to 50 μ m, and the thickness of the sustain-side bus electrodes and the scan-side bus electrodes causes a raised portion of thickness 2 to 50 μ m to be formed on the surface of an insulating layer provided on said front substrate.

86. (New) The plasma display panel according to claim 52, comprising a metal electrode connecting the sustain-side bus electrodes to each other.

87. (New) The plasma display panel according to claim 52, comprising a transparent electrode connecting the sustain-side bus electrodes to each other.

88. (New) The plasma display panel according to claim 52, wherein the

sustain-side bus electrodes are connected to each other to act as an integrated common bus electrode.

89. (New) The plasma display panel according to claim 88, wherein resistance of the common bus electrode is $1/3$ to $1/12$ of that of the scan-side bus electrodes.

90. (New) The plasma display panel according to claim 88, wherein the common bus electrode has a thickness of 10 to 50 μm , and the thickness of the common bus electrode causes a raised portion of thickness 2 to 50 μm to be formed on the surface of an insulating layer provided on said front substrate.

91. (New) The plasma display panel according to claim 52, comprising a metal electrode connecting the scan-side bus electrodes to each other.

92. (New) The plasma display panel according to claim 52, comprising a transparent electrode connecting the scan-side bus electrodes to each other.

93. (New) The plasma display panel according to claim 52, wherein the scan-side bus electrodes are connected to each other to act as an integrated common bus electrode.

94. (New) The plasma display panel according to claim 52, wherein the resistance of the common bus electrode is $1/3$ to $1/12$ of that of the sustain-side bus electrode.

95. (New) The plasma display panel according to claim 93, wherein the common bus electrode has a thickness of 10 to 50 μm , and the thickness of the common bus electrode causes a raised portion of thickness 2 to 50 μm to be formed on the surface of an insulating layer provided on said front substrate.

96. (New) The plasma display panel according to claim 52, wherein the distance between the neighboring scan electrodes or the neighboring scan-side bus electrodes on vertically neighboring pixel cells is 20 to 200 μm .

97. (New) The plasma display panel according to claim 52, wherein the distance between the neighboring sustain electrodes or the neighboring sustain-side bus electrodes on vertically neighboring pixel cells is 20 to 200 μm .